What is claimed is:

1. A test kit for a semiconductor package comprising:

a pick-and-place tool structured to load/unload the semiconductor package;

a head assembly including a package guider for aligning the semiconductor package falling from the pick-and-place tool, and a socket guider for pressing a socket cover at an edge of the package guider before the package guider operates and for performing a pre-alignment function for an operation of the package guider when the socket guider contacts the socket cover; and

a socket which is positioned under the head assembly and connects the semiconductor package loaded by the pick-and-place tool and the head assembly to a tester.

2. The test kit for the semiconductor package of claim 1, wherein the socket includes:

the socket cover positioned on an uppermost portion of the socket and to be used in the pre-alignment function performed by the socket guider of the head assembly;

a socket contact board positioned under the socket cover and having a plurality of socket pins arranged in an array pattern and for electrically connecting to the external connection terminals of the semiconductor package; and

a latch positioned on the socket contact board, the latch structured to be opened by a pressing force of the package guider, the latch allowing the semiconductor package to be loaded/unloaded and fixing the semiconductor package when the pressing force of the package guider is removed.

3. The test kit for the semiconductor package of claim 2, wherein the socket contact board is a universal socket contact board capable of receiving more than one type of semiconductor package.

4. The test kit for the semiconductor package of claim 1, wherein the socket further includes a free-sized adapter formed on the socket contact board.

5. The test kit for the semiconductor package of claim 4, wherein the free-sized adapter is structured to ensure a space for positioning the package guider when the external

connection terminals of the semiconductor package are connected to the socket pins of the socket contact board and to protect surfaces of the socket contact board.

6. The test kit for the semiconductor package of claim 5, wherein the free-sized adapter includes a support portion and an opening.

7. The test kit for the semiconductor package of claim 5, wherein the free-sized adapter is made of a flexible plastic material.

8. The test kit for the semiconductor package of claim 1, wherein the pick-and-place tool is structured to pick a body of the semiconductor package by a vacuum force and to load/unload the semiconductor package.

9. The test kit for the semiconductor package of claim 1, wherein the head assembly is structured to load/unload a plurality of semiconductor packages simultaneously.

10. The test kit for the semiconductor package of claim 1, wherein the package guider of the head assembly includes:

inclined portions which are formed at four corners of the package guider, the semiconductor package body sliding while contacting one or more of the inclined portions and being aligned; and

an alignment portion in which the semiconductor package sliding along one or more of the inclined portions falls in an aligned state.

11. The test kit for the semiconductor package of claim 1, wherein corners of the socket cover slide along one or more of inclined surfaces formed at ends of the socket guider when the socket cover is pressed and are inserted into the socket guider so that the socket guider performs an alignment function of matching a position of the head assembly with a position of the socket.

12. The test kit for the semiconductor package of claim 1, wherein the socket is used in an interface board for a parallel test of semiconductor packages.

13. The test kit for the semiconductor package of claim 1, wherein the socket is used in an interface board for a burn-in test of semiconductor packages.

14. A method for testing a semiconductor package comprising:

performing a first alignment by docking a socket guider of a head assembly on a socket cover of one of a plurality of sockets on an interface board;

opening a latch of the socket by pressing the socket cover using a package guider of the head assembly;

performing a second alignment of the semiconductor package that is loaded in a pick-and-place tool with the package guider;

mounting the semiconductor package on a socket contact board formed inside the socket;

affixing the semiconductor package by the latch by removing pressing force from the package guider;

separating the semiconductor package from the pick-and-place tool; and

performing an electrical test for the semiconductor package mounted on the socket contact board.

15. The method of claim 14, wherein the electrical test for the semiconductor package is a parallel test.

16. The method of claim 14, wherein the interface board is used for a final test of the semiconductor package.

17. The method of claim 16, wherein the final test is any one of high temperature, room temperature, and low temperature tests.

18. The method of claim 14, wherein the interface board is used for a burn-in test of the semiconductor package.

19. The method of claim 14, wherein the first alignment includes four corners of the socket guider contacting four corners of the socket cover.

20. The method of claim 14, wherein the pick-and-place tool loads and unloads the semiconductor packages by presence or absence of a vacuum force.

21. The method of claim 14, wherein performing the second alignment comprises:

positioning a semiconductor package that is sliding along inclined portions of the package guider in a correct position; and

passing the semiconductor package that is positioned in the correct position through an alignment portion.

22. The method of claim 14, wherein the socket contact board further includes a structure to ensure a space for positioning the package guider when the semiconductor package is loaded, and to protect a surface of the socket contact board.

23. The method of claim 22, wherein the structure is a free-sized adapter having a general structure that can be applied irrespective of a type of an external connection terminal of the semiconductor package.

24. The method of claim 14, wherein the latch fixes the semiconductor package by pressing an upper portion of the semiconductor package.

25. The method of claim 14, wherein the semiconductor package uses solder balls as the external connection terminals.